

**REMARKS**

Claims 4 and 11-15 are pending. Claims 4, 12, 14 and 15 have been amended. Claims 11-14 are independent.

In the Office Action, the Examiner incompletely acknowledged the Information Disclosure Statement ("IDS") dated May 3, 2001. That is, the Examiner did not initial the Japanese reference, for which an English abstract was provided, instead marking it with an asterisk. From the handwritten message at the bottom of the Office Action Summary, it appears that upon submission of a duplicate copy of the previously-cited Japanese reference, the Examiner will initial the reference. In view of the foregoing, submitted herewith is the requested duplicate copy of JP 10-004350 and the English Abstract thereof, that was originally submitted with the IDS. It is requested that the reference be initialed and the PTO-1449 be returned with the next Office Action.

Claims 4 and 15 were objected to due to an informality. In particular, PLL was inadvertently typed "PLI." The above amendment to those claims corrects this informality. Withdrawal of the objection is requested.

Claims 11 and 12 were rejected under 35 U.S.C. § 102(e) over U.S. Patent 5,900,784 (O'Sullivan). Claims 4 and 13-15 were rejected under 35 U.S.C. § 103 over O'Sullivan in view of U.S. Patent 6,147,532 (Ueda) and further in view of U.S. Patent 5,986,514 (Salvi et al.). Applicant submits that the independent claims are patentable for at least the following reasons.

Claims 11 and 13, both require a PLL frequency synthesizer circuit wherein "when the control voltage changes to a value close to one of the driving limits, the power supply voltage is modified independently of the control voltage so as to maintain the stability of the output signal from the VCO." Amended claims 12 and 14 both require the use of the

PLL frequency synthesizer wherein "the power supply signal (applied to the VCO) is controlled independently of the control signal to thereby widen an apparent lock range of the PLL." Claim 4 depends from claim 12 and claim 15 depends from claim 14 and include all of the respective limitations found therein.

O'Sullivan adjusts a bias voltage of a reference signal  $V_{in}$  to adjust for temperature and power supply variations to maintain lock. Col. 5, lines 45 through 47. There is no teaching whatsoever in O'Sullivan of modifying the power supply voltage (or signal), still less of modifying it independently of the control voltage (or signal), to maintain stability of the output of the VCO, as in claims 11 and 13, or to widen the apparent lock range of the PLL, as in claims 12 and 14. In fact, O'Sullivan teaches that the control voltage for the VCO, namely  $V_{in}$ , is controlled by application of a bias voltage at least in part on the basis of power supply variations.

Thus, the control voltage and the power supply voltage in O'Sullivan are not independent of one another, and there is certainly no teaching of modifying the power supply voltage, independently of the control voltage. Further, O'Sullivan does not teach modifying the power supply voltage, only that it may vary, which is not the same thing. For at least these reasons, the power supply voltage in O'Sullivan is: (1) *not* modified (but may vary); and (2) *not* independent of the control voltage, since as the power supply varies, the control voltage  $V_{in}$  will be varied. Therefore, claims 11-14 are believed clearly distinguished from O'Sullivan.

Neither Ueda nor Salvi et al. remedy the above-mentioned deficiencies of O'Sullivan as a reference against the independent claims.

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In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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